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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,624	06/30/2000	Stephen Jourdan	2207/8609	9451

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 08/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/608,624	Applicant(s) JOURDAN ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/30/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-11 and 15-19* is/are rejected.

7)☒ Claim(s) *8 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/30/00* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4/5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

at page 6, line 1, "4(a)" should read -4(b)-; and

Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-3 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims recite nothing more than a nonstatutory subject matter.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material. "Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, 1).

Note the claimed invention, a trace, is just a general term describing a physical or logical path; or a sequence of instructions, as defined at page 1, lines 15-17 in the specification. The examiner submits that the claims are abstract ideas or the mere manipulation of abstract ideas, or the mere arrangements of data.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Arbabi et al. (US 5,461,699) (Herein referred as Arbabi et al.)

Referring to claim 1, Arbabi et al., as claimed, discloses: a trace having a multiple-entry (X0, X1, …, Xn, see Fig. 9), single exit (Y, see Fig. 9) architecture.

As to claim 2, Arbabi et al. also discloses: the trace being a complex trace having multiple independent prefixes (W01, W11, …, Wn1, see Fig. 9) and a common, shared suffix (b1, see Fig. 9). Note the other paths are not considered when the values (such as w02, w12, …, wn2, and b0, b2, and b3) thereof are zero as shown in Fig. 9.

As to claim 3, Arbabi et al. also discloses: the trace being indexed by an address (note X0, X1, … Xn, see Fig. 9, are best reasonably and broadly interpreted as the logical addresses) of a terminal instruction therein.

6. Claims 4-7, 9-11, and 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Black et al., "The Block-base Trace Cache", ACM SIGARCH Computer Architecture News, Proceedings of the 26th annual international symposium on computer architecture, May 1999. (Herein referred as Black et al.)

Referring to claim 4, Black et al. discloses, as claimed, a front-end system for a processor, comprising: an instruction cache system (I-Cache, See Fig. 2), an extended block cache system (See Fig. 2), comprising: a fill unit (Fill Unit, See Fig. 2) provided in communication with the instruction cache system, a block cache (Block Cache, See Fig. 2), and a selector (Fetch Buffer, see Fig. 2) coupled to the output of the instruction cache system (I-Cache, See Fig. 2) and to an output of the block cache (Block Cache, See Fig. 2).

As to claim 5, Black et al. also discloses: a block predictor (Trace Table, see Fig. 2, and Section 3.1, first paragraph, mentioning "the trace table can also be viewed as part of the next trace predictor") provided in communication with the fill unit and the block cache as shown in Fig. 2.

As to claim 6, Black et al. also discloses: the block cache being to store traces having a multiple-entry (see Fig. 2, and

Section 3.2, first paragraph, mentioning "the block cache stores aligned instruction blocks. To support multiple simultaneous accesses, the block cache is replicated."), single exit (the output from Final Collapse which is the input to Fetch Buffer, see Figs. 2 and 4) architecture.

As to claim 7, Black et al. also discloses: the block cache is to store complex traces having multiple independent prefixes (see Fig. 2, and Section 3.2, first paragraph, mentioning "the block cache stores aligned instruction blocks. To support multiple simultaneous accesses, the block cache is replicated.") and a common suffix (the output from Final Collapse which is the input to Fetch Buffer, see Figs. 2 and 4).

Referring to claim 9, Black et al. discloses as claimed comprising: predicting an address (the predicted trace-id, see Fig. 2, and Section 3.1, first paragraph, mentioning "the trace table can also be viewed as part of the next trace predictor. The next trace predictor uses block-id execution history and branch history bits to generate the predicted trace-id which is used to access the trace table.") of a terminal instruction of an extended block to be used, determining whether the predicted address matches an address of a terminal instruction of a previously created extended block, and selecting one of the

extended block in the event of a match (see also section 3.2.1 about block cache read).

As to claim 10, Black et al. also discloses: creating a new extended block when there is no match (see section 3.2.2 about block cache fill).

As to claim 11, Black et al. also discloses: receiving new instructions until a terminal condition occurs (certainly and inherently existing in the Black et al.'s system since the terminal condition is a boundary of the instruction sequence), assembling the new instructions into an extended block, determining whether an address of a terminal instruction in the new block matches an address of a terminal instruction of a pre-existing block, and unless a match occurs, storing the new block in a memory (see section 3.2.1 about block cache read, and section 3.2.2 about block cache fill).

As to claim 15, Black et al. also discloses: outputting instructions of the selected block for execution (see Fig. 2; the instruction inputs to execution core).

Referring to claim 16, Black et al. discloses as claimed comprising: a front end stage to store multiple-entry (see Fig. 2, and Section 3.2, first paragraph, mentioning "the block cache stores aligned instruction blocks. To support multiple

simultaneous accesses, the block cache is replicated."), single exit (the output from Final Collapse which is the input to Fetch Buffer, see Figs. 2 and 4) traces (inside Block Cache, See Fig. 2), and an execution unit (the execution core, see Fig. 2) in communication with the front end stage.

As to claim 17, Black et al. also discloses: the front-end stage comprises: an instruction cache system (I-Cache, See Fig. 2), an extended block cache system, comprising: a fill unit (Fill Unit, See Fig. 2) provided in communication with the instruction cache system (I-Cache, See Fig. 2), a block cache (Block Cache, See Fig. 2), and a selector (Fetch Buffer, see Fig. 2) coupled to the output of the instruction cache system (I-Cache, See Fig. 2) and to an output of the block cache (Block Cache, See Fig. 2).

As to claim 18, Black et al. also discloses: the block cache (Block Cache, See Fig. 2) being to store the multiple-entry, single exit traces (as set forth above in the rejection to claim 6).

As to claim 19, Black et al. also discloses: the extended block cache system further comprises a block predictor (Trace Table, see Fig. 2, and Section 3.1, first paragraph, mentioning "the trace table can also be viewed as part of the next trace predictor") provided in communication with the fill unit and the block cache (as set forth above in the rejection to claim 5).

Allowable Subject Matters

7. Claims 8, and 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Arbabi et al. and Black et al., the closest references, do not teach or fairly suggest a front-end system comprising: the extended block cache system having a block predictor to store masks associated with the complex traces, the masks distinguishing the prefixes from each other (claim 8); the storing comprising, when an older block causes a match, storing the new block over the old block in a memory if the old block is subsumed within the new block (claim 12); the storing comprising, when an older block causes a match, dropping the new block if the new block is subsumed within the older block (claim 13); and the storing comprising, when an older block causes a match, creating a complex block if the new block and the older block share a common suffix but include different prefixes (claim 14).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, such as Bala'678; Kranich et al.'675; and Breternitz, Jr. et al.'999 teaching the similar limitations as claimed.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:**

Official faxes: 703-746-7239; and

After Final faxes: 703-746-7238;

Customer Service faxes: 703-746-7240.

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HENRY W. H. TSAI
PRIMARY EXAMINER

August 11, 2003